Figure 1

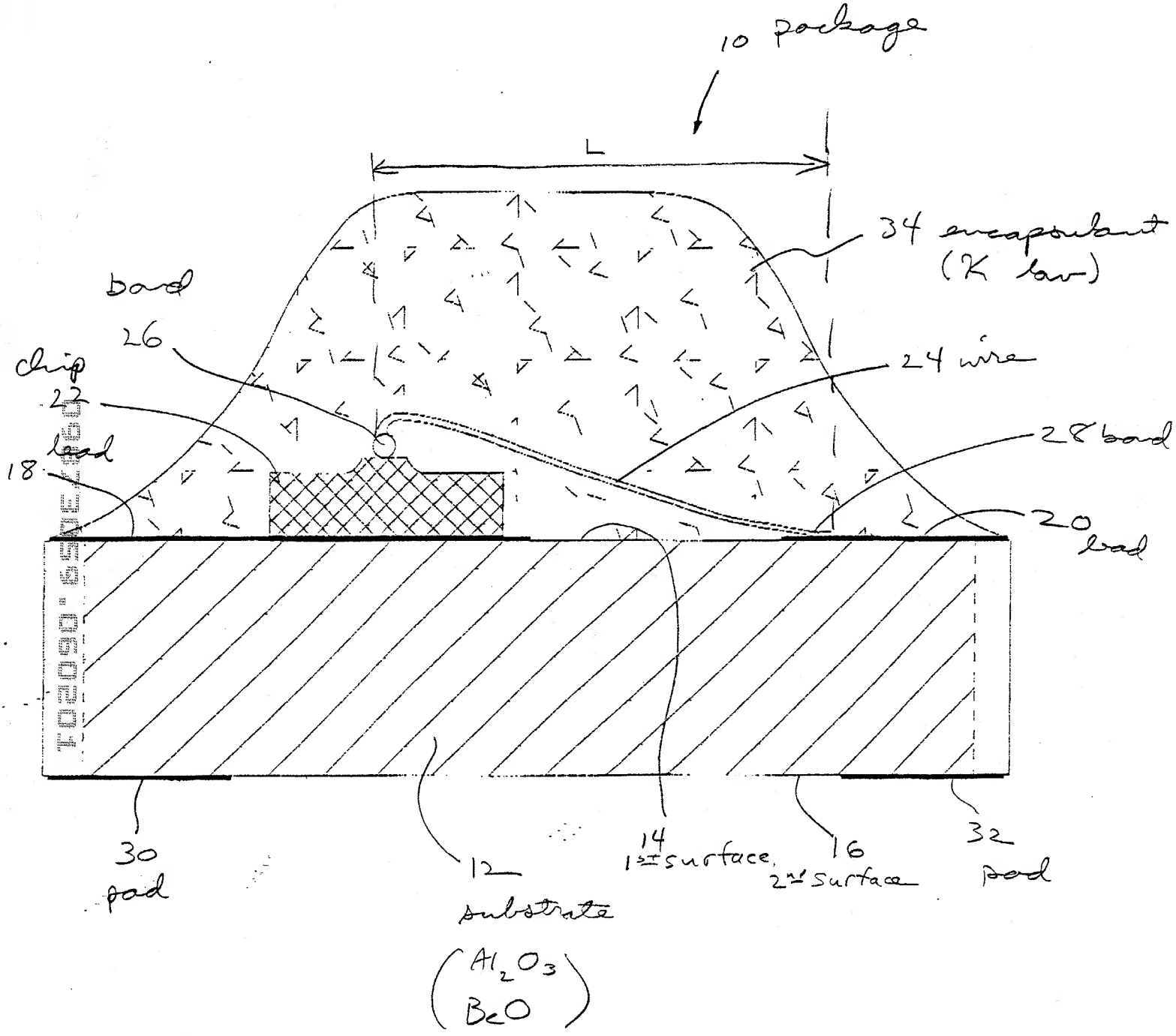

10 package
L
34 encapsulant (K bar)
bond
26
chip
22
lead
18
24 wire
28 bond
20 bond
package edge
30
pad
12
substrate
(Al_2O_3 / BeO)
14
1st surface
16
2nd surface
32
pad

Fig. 2 Top

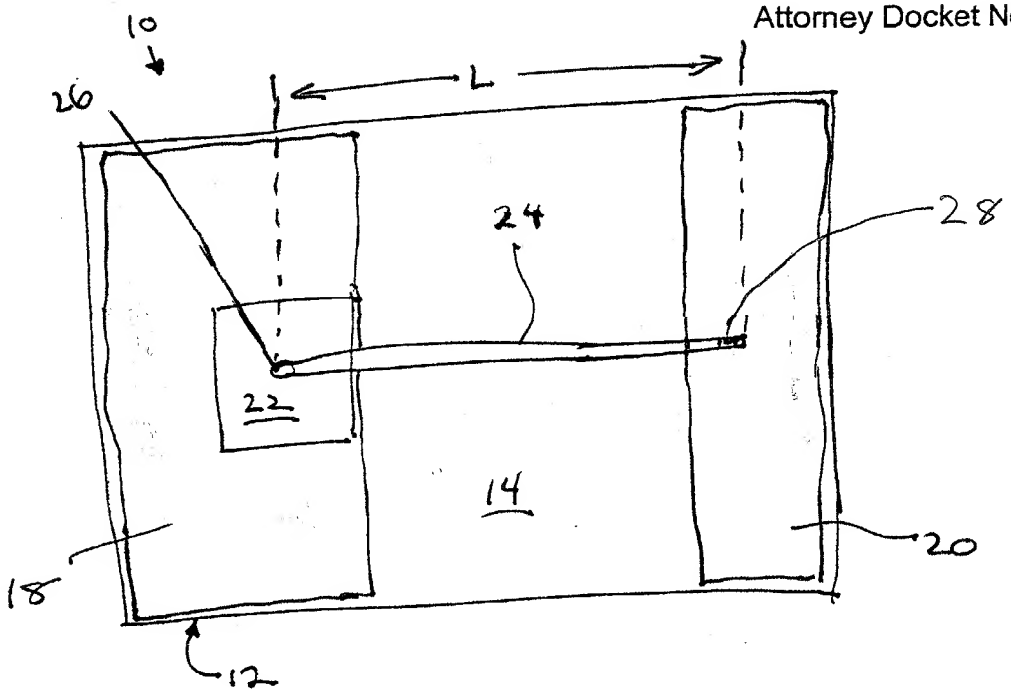
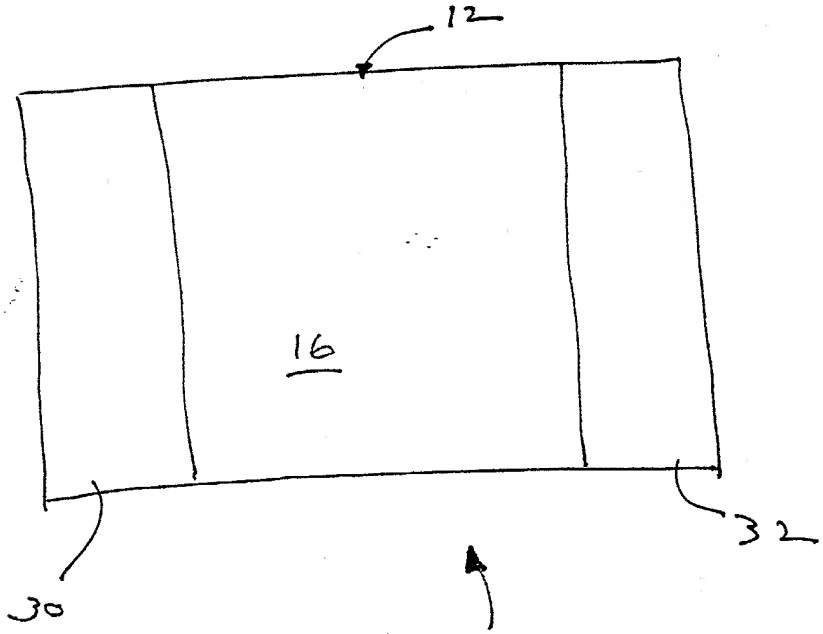


Fig. 3 Bottom



T:\2006\06-0595\06-0595.DOC

Fig. 4

Top perspective view showing multiple chip (22) implementation

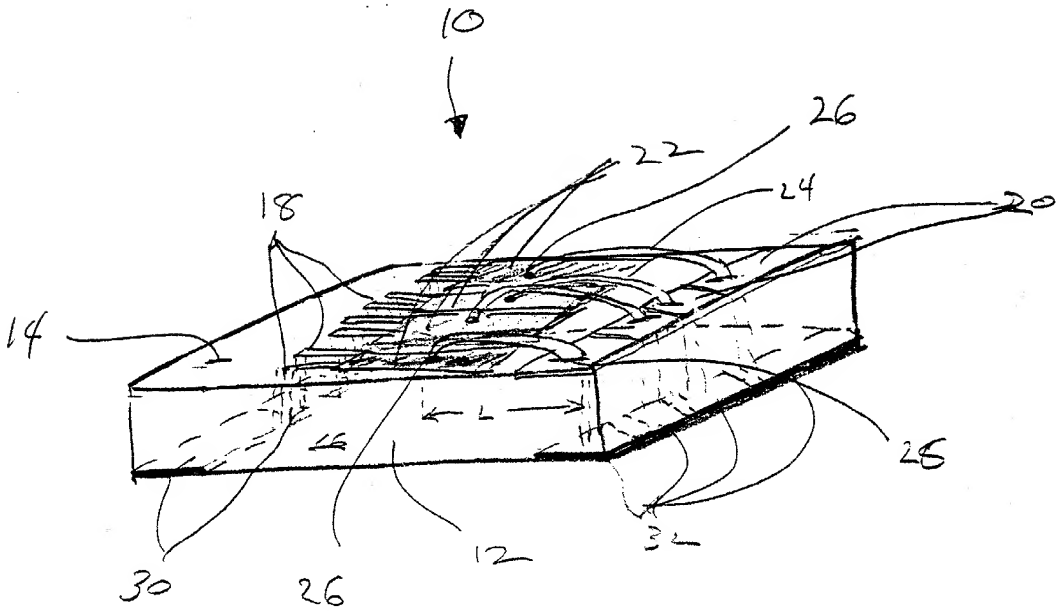
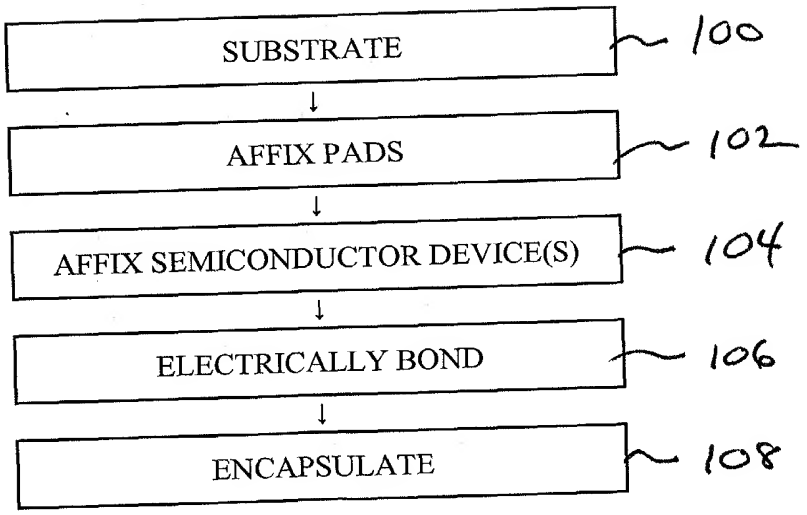


FIGURE 5


SUBSTRATE
100
AFFIX PADS
102
AFFIX SEMICONDUCTOR DEVICE(S)
104
ELECTRICALLY BOND
106
ENCAPSULATE
108